

wordline may be sensed in parallel allows the time to be amortized over all of the memory cells of a wordline such that the average time to access the data of each memory cell is significantly reduced over the prior art. Under this scheme no drain bias circuit is required because no cell current is required. Similarly, a differential sense amplifier is also not required. Because, the value of the read voltage V_G and the maximum swing of the threshold voltage V_t are known, an analog to digital converter may be used to convert the voltage of a bitline into a digital value, therefore not requiring a sense amplifier.

FIG. 10 shows the periphery circuitry 80 of the memory device 70 for one embodiment. Periphery circuitry 80 generally comprises voltage regulation circuitry 205, voltage switches 210, row and column decoders 215, and sensing circuitry 220.

Periphery circuitry 80 is also shown as including an optional control engine 200 that includes a read algorithm "R" 201 and a write algorithm "W" 202 that control engine 200 uses to control the periphery circuitry 80 for accessing the memory cell array 75. Control engine 200 may alternatively be provided externally to the memory device 70. Control engine 200 is coupled to receive the address and control signals such that it can appropriately control the voltage regulation circuitry 205, voltage switches 210, and the row and column decoders 215.

The voltage regulation circuitry 205 is coupled to receive the external supply voltages V_{CC} , V_{PP} , and V_{SS} . Typically, values of V_{CC} and V_{PP} are 5 volts and 12 volts, respectively. However, for some embodiments V_{CC} and V_{PP} may be the same voltage, (e.g. 5.0 volts or 3.3 volts). The voltage regulation circuitry 205 may include charge pumps, DC-to-DC converters, and/or voltage dividers for producing the read voltage V_G and the source voltage V_s .

The voltage switches 210 are coupled to the voltage regulation circuitry 205 and to the wordlines, bitlines, and source straps of memory cell array 75. Voltage switches 210 selectively provides the desired voltages (e.g. source voltage V_s) to the memory cell array in response to control signals provided by the control engine 200.

The row decoders of row and column decoders 215 are coupled to the voltage switches 210 for receiving the read voltage V_G and supplying the read voltage V_G to a wordline of memory cell array 75 indicated by the address lines ADDR. As previously mentioned, column decoders are optional and may be used merely to multiplex sensing circuitry 220 to sense specific subsets of bitlines 120-122 of the memory cell array 75. If no column decoders are provided, sensing circuitry 220 will sense all of the bitlines of the memory cell array 75 in parallel.

Sensing circuitry 220 is shown as including analog to digital converter "ADC" 221 that translates the voltages sensed at bitlines 120-122 to digital values. Sensing circuitry 220 may include latches for storing the sensed voltages such that all of the voltages on bitlines 120-122 may be dumped into the latches and sequentially output in smaller subsets to data bus 85.

The memory device architecture shown in FIGS. 7-10 illustrate a nonvolatile memory device having a page mode read operation. If latches or another form of memory are provided in sensing circuitry 220, an entire wordline of memory cells may be stored in a cache-like fashion wherein a wordline of data is fetched at a time from memory cell array 75. Subsequent accesses to memory cell array 75 are done entirely within a buffer memory of sensing circuitry

220 (not shown) using row and column decoders 215. Subsequent accesses will continue to be made to the buffer memory of sensing circuitry 220 instead of memory cell array 75 until data is attempted to be fetched from memory cell array 75 that is not stored in sensing circuitry 220.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention. The specification and drawings are, accordingly, to be regarded in an illustrative rather than restrictive sense.

What is claimed is:

1. A method for determining data stored by a memory cell having a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor, comprising the steps of:

floating the bitline;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell; and

sensing the third voltage to determine the data stored by the memory cell.

2. The method of claim 1, further comprising an initial step of setting the bitline to a ground potential.

3. The method of claim 1, wherein the memory cell is a nonvolatile memory cell.

4. A method for simultaneously determining data stored by a plurality of memory cells each having a select gate coupled to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor, comprising the steps of:

floating the plurality of bitlines;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells; and

sensing the plurality of third voltages to determine the data stored by the plurality of memory cells.

5. The method of claim 4, further comprising an initial step of setting the plurality of bitlines to a ground potential.

6. The method of claim 4, wherein the plurality of memory cells are nonvolatile memory cells.

7. The method of claim 4, wherein determining the data stored by the plurality of memory cells comprises reading a page of data.

8. A method for determining data stored by a memory cell having an adjustable threshold voltage, a select gate coupled to a wordline, a first electrode coupled to a bitline, and a second electrode coupled to a conductor, comprising the steps of:

floating the bitline;

applying a first voltage to the wordline;

applying a second voltage to the conductor such that the bitline is set to a third voltage;

determining the adjustable threshold voltage of the memory cell based on the third voltage; and

determining the data stored in the memory cell based on the adjustable threshold voltage of the memory cell.

9. A memory device comprising:

a memory array having data stored in a memory cell, the memory cell having a select gate coupled to a wordline,

a first electrode coupled to a bitline, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the bitline is set to a third voltage that is equal to the first voltage minus a threshold voltage of the memory cell, wherein the periphery circuit senses the third voltage to determine the data stored by the memory cell.

10. The memory device of claim 9, wherein the periphery circuit further transmits a ground potential to the bitline before transmitting the first voltage or the second voltage to the memory cell.

11. The memory device of claim 9, wherein the memory cell is a nonvolatile memory cell.

12. The memory device of claim 9, wherein the periphery circuit comprises:

a voltage regulation circuit outputting the first voltage and the second voltage;

a voltage switching circuit coupling the second voltage to the memory cell; and

a sensing circuit coupled to the memory cell, wherein the sensing circuit senses the third voltage to determine the data stored by the memory cell.

13. The memory device of claim 12, further comprising: a decoder circuit receiving the first voltage from the voltage switching circuit and coupling the first voltage to the memory cell, the decoder circuit decoding a location of the memory cell in the memory array.

14. The memory device of claim 12, further comprising: a control circuit having read circuitry and write circuitry, each coupled to the voltage regulation circuit, the voltage switching circuit, and the sensing circuit, wherein the control circuit controls when the first voltage and the second voltage are supplied to the memory cell and when the third voltage is sensed by the sensing circuit.

15. The memory device of claim 12, wherein the sensing circuit comprises:

an analog-to-digital converter circuit operative to receive the third voltage and generate a digital value.

16. A memory device comprising:

a memory array having data stored in a plurality of memory cells, the plurality of memory cells each having a select gate coupled to a wordline, a first electrode coupled to one of a plurality of bitlines, and a second electrode coupled to a conductor; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a first voltage to the wordline and transmitting a second voltage to the conductor such that the plurality of bitlines is set to a plurality of third voltages, wherein one of the plurality of third voltages is equal to the first voltage minus a threshold voltage of one of the plurality of memory cells, and wherein the periphery circuit simultaneously senses the plurality of third voltages to determine the data stored by the memory array.

17. A memory device comprising:

a memory array having data stored in a memory cell having an adjustable threshold voltage; and

a periphery circuit coupled to the memory array, the periphery circuit transmitting a plurality of voltages to the memory cell and sensing the adjustable threshold voltage of the memory cell to determine the data stored by the memory cell.

18. A memory device comprising:

means having an adjustable threshold voltage for storing data; and

means coupled to the storing means for determining the data stored in the storing means by sensing the adjustable threshold voltage.

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